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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,546	09/19/2003	Takeshi Ashida	9319S-000548	5558

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EXAMINER	
EDMONDSON, LYNNE RENEE	
ART UNIT	PAPER NUMBER
1725	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,546	ASHIDA, TAKESHI	
	Examiner	Art Unit	
	Lynne Edmondson	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/10/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 5-13 are rejected under 35 U.S.C. 102(a) as being anticipated by Abbott et al. (USPN 6337445 B1).

Abbott teaches a mask and method of producing an electronic device (col 1 lines 13-23 and col 2 lines 43-53) by applying solder to terminals of a substrate though openings in a mask (stencil) wherein the openings are larger than substrate terminals (col 3 line 58 – col 4 line 27 and col 5 lines 39-61) and subjecting the solder to reflow conditions (figures 8, 10, 11a and 11b, col 9 lines 22-40 and col 10 line 13 – col 11 line 10). It is noted that a variety of electronic components can be made by this method and that opto-electronic components can be made using other methods.

3. Claims 5-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaynes et al. (USPN 6165885).

Gaynes teaches a mask and method of producing an electronic device such as a diode (col 11 lines 1-7) by applying solder to terminals of a substrate though openings in a mask wherein the openings are larger than substrate terminals (figures 76 and 77 and col 20 lines 9-65) and subjecting the solder to reflow conditions (figure 2) . Solder covers the conductive region, which includes a wiring line (figures 22-26 and 33). It is noted that a variety of electronic components can be made by this method and that opto-electronic components can be made using other methods.

4. Claims 5-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Grigg (USPN 6622380 B1).

Grigg teaches a mask and method of producing an electronic device (col 2 lines 51-67) by applying solder to terminals of a flexible substrate (col 4 lines 8-19) though openings in a mask (30) wherein the openings are larger than substrate terminals (figures 3A and 36). Solder is applied through the mask (col 4 line 53 – col 5 line 4) and subjected to reflow conditions (col 4 lines 20-50 and col 5 lines 5-29). Solder covers the conductive region which includes a wiring line (traces 12, figure 3B).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grigg (USPN 6622380 B1) in view of Ishibashi (USPN 5931577).

Grigg teaches a mask and method of producing an electronic device (col 2 lines 51-67) by applying solder to terminals of a flexible substrate (col 4 lines 8-19) though openings in a mask (30) wherein the openings are larger than substrate terminals (figures 3A and 36). Solder is applied through the mask (col 4 line 53 – col 5 line 4) and subjected to reflow conditions (col 4 lines 20-50 and col 5 lines 5-29). Solder covers the conductive region, which includes a wiring line (traces 12, figure 3B). However there is no disclosure of forming opto-electronic devices.

Ishibashi teaches formation of opto-electronic devices (light emitting diodes) by screening solder paste and reflow soldering the parts (col 4 line s32-57) as is conventional in the art.

It would have been obvious to one of ordinary skill in the art at the time of the invention that a variety of electronic components can be made by this method including but not limited to opto-electronic devices.

Response to Arguments

7. Regarding applicant's argument that Gaynes does not teach mounting a package on a substrate through solder see figures 4-9, col 18 lines 4-34col 20 lines 9-56 and col 22 line 35 – col 23 line 61 which teach this process including a reflow step.

Therefore the 102 rejection of claims 5-13 as anticipated by Gaynes stands.

8. Regarding applicant's argument that Grigg does not teach placing a mask on a substrate of a flexible board and applying solder through the mask, see col 4 lines 13-16 which teach a flexible substrate to which a mask (30) is applied (col 4 lines 30-40). Solder is applied through the mask (col 4 line 53 – col 5 line 4).

Therefore the 102 rejection of claims 5-9 as anticipated by Grigg stands.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Asai (US 2004/0212030 A1) and Glenn et al. (USPN 6564454 B1).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne Edmondson whose telephone number is (571) 272-1172. The examiner can normally be reached on Monday through Thursday from 6:30 a.m. to 5 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Dunn can be reached on (571) 272-1171. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lynne Edmondson
Primary Examiner
Art Unit 1725

LRE

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3/29/05